



**Government of Karnataka
Department of Technical Education**

C-25 Diploma in Electronics & Communication Engineering

Scheme of Studies

(Effect from the AY 2025-26)



Government of Karnataka
DEPARTMENT OF TECHNICAL EDUCATION

Curriculum Structure

I Semester Scheme of Studies

Sl. No.	Teaching Department	Course Code	Course Name	Hours per week			Total Contact Hours/week	Credits	CIE Marks		Theory SEE Marks		Practice SEE Marks		Total Marks
				L	T	P			Max	Min	Max	Min	Max	Min	
Integrated Courses															
1	SC	25SC11I	Engineering Mathematics-I	4	0	4	8	6	50	20	50	20	-	-	100
2	CS	25CS01I	IT Skills	3	0	4	7	5	50	20	-	-	50	20	100
3	EE/EC	25EE01I	Fundamentals of Electrical & Electronics Engineering.	3	0	4	7	5	50	20	-	-	50	20	100
4	EC	25EC11I	Digital Electronics-I	4	0	4	8	6	50	20	50	20	-	-	100
Audit Course															
5	EC	25EC12I	Environmental Sustainability	2	0	0	2	2	50	20	-	-	-	-	50
6	Personality Development		NCC/NSS/YOGA/SPORTS...	Students are expected to engage in any one of these activities from 1 st semester to 6 th semester(No Credits)											
Total				16	0	16	32	24	250	-	100	-	100	-	450

Note: The course 25EE01I shall be taught by faculty from the Electrical & Electronics (E&E) department. In the event that E&E faculty are not available in the institution, the course 25EE01I shall be assigned to faculty from the Electronics & Communication (E&C) department. If both E&E and E&C departments exist in the institution, the course 25EE01I shall be taught by the E&C faculty.



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DEPARTMENT OF TECHNICAL EDUCATION

Program	Electronics and Communication Engineering	Semester	1
Course Name	Digital Electronics-I	Type of Course	Integrated
Course Code	25EC11I	Contact Hours	8 hours/week (104 hours/semester)
Teaching Scheme	L: T:P :: 4:0:4	Credits	6
CIE Marks	50	SEE Marks	50 (Theory)

1. Rationale:

Digital electronics stems from its inherent advantages in reliability, versatility, scalability, and integration, reflecting its critical role in modern technology. Digital systems have transformed various industries, leading to advances in computing, communication and automation, making it a fundamental aspect of contemporary engineering and technology.

2. Course Outcomes: At the end of the Course, the student will be able to:

CO-01	Understand and perform arithmetic and conversion operations on different number systems.
CO-02	Formulate, simplify and implement simple logic functions using logic gates.
CO-03	Build and analyze various combinational circuits in a real time environment.
CO-04	Identify and utilize the suitable ICs for different applications.

3. Course Content

WEEK	CO	PO	Theory	Practice
1	1	1,2	<p>Introduction to Digital Electronics, Importance, and Its applications. https://youtu.be/DBTna2ydmC0?feature=shared</p> <p><u>Number Systems</u></p> <ul style="list-style-type: none">• Comparison between analog and digital signals with real-world examples.• Number systems: Binary, Decimal and Hexadecimal. Relevance and examples.	<ol style="list-style-type: none">1. Demonstrate number system and its conversion by using scientific calculator and verify theoretically.2. Familiarize Digital IC Trainer Kit and do the following,<ul style="list-style-type: none">☒ Precautions to be taken while handling ICs.☒ Analyze Pin diagram of an IC.☒ Demonstrate the testing of an IC using an IC tester.

			<p>https://youtu.be/FFDMzbrEXaE?feature=shared</p> <p><u>Conversion between number systems with examples</u></p> <ul style="list-style-type: none"> • Binary to decimal and vice versa. • Hexadecimal to decimal and vice versa. • Binary to hexadecimal and vice-versa (bitwise grouping only). 	<p>☐ Demonstrate equivalent analog voltages for positive logic of logic 0 and logic 1 using Multimeter</p>
2	1,4	1,2	<p><u>Arithmetic operations and Codes</u></p> <ul style="list-style-type: none"> • Arithmetic operations. <ul style="list-style-type: none"> ☐ Addition and Subtraction on 4 bit and 8 bit binary numbers with examples (integers only). ☐ Addition and subtraction of Hexadecimal numbers. • 1's & 2's complement of binary numbers with examples. • Representation of signed binary numbers. Problems on subtraction using 2's complement. • Codes: BCD, Gray and ASCII- its features with examples, applications 	<ol style="list-style-type: none"> 1. Perform BCD addition with simple examples. 2. Develop Binary to Gray code converter using IC 7486 and vice -versa.
3	4	2,5	<p><u>Digital Integrated Circuits</u></p> <p>https://study.com/academy/lesson/video/digital-integrated-circuits-definition-types-examples.html</p> <ul style="list-style-type: none"> • IC: Concept, Classification-Based on Scale of Integration. • IC- advantages and disadvantages • Logic-family concept, need and types of logic families. • Logic-family definitions: Propagation delay, fan-out, fan-in, power dissipation, noise margin, speed and speed-power product. 	<ol style="list-style-type: none"> 1. Verify the functionality of all the logic gates in the following ICs. <ol style="list-style-type: none"> a. 7432 b. 7408 2. Tabulate the parameters: Propagation delay, fan-out, fan-in, power dissipation, noise margin of the following ICs as per their Data Sheet. <ol style="list-style-type: none"> a. 7404 b. 7486
4	2,4	1,2	<p><u>Boolean Algebra and Logic Gates:</u></p> <ul style="list-style-type: none"> • Boolean algebra: Understanding of Constants, variables, functions with examples. • Boolean identities and Boolean Laws. • Logic-gates (NOT, OR, AND, NOR, NAND, EX-OR and EX-NOR) Symbol, function, expression and truth-table. • De-Morgan's Theorems with proof and examples. 	<ol style="list-style-type: none"> 1. Verification of Truth Table for all the logic gates. 2. Verify De-Morgan's Theorems using Logic gates.

5	2,4	1,2	<u>Universal Logic Gates & Boolean expression simplification</u> <ul style="list-style-type: none"> • Universal Logic Gates: Concept, examples. • Realization of all logic gates using NAND Gate. • Simplification of Boolean expressions using Boolean algebra. • Build the logic circuit using logic gates for simplified Boolean expression. 	<ol style="list-style-type: none"> 1. Realization of NOT, OR, AND gates using NOR Gates. 2. Realization of NAND, EX-OR, EX-NOR gates using NOR Gates.
6	2,4	1,2	<u>Boolean expression forms & conversions</u> <ul style="list-style-type: none"> • SOP and POS forms: Conversion into standard SOP forms. • Conversion into standard POS forms. • Translate SOP and POS expressions into truth-table. • Convert truth-table to SOP and POS expressions. 	<ol style="list-style-type: none"> 1. Simplify a given SOP (3 variable) using Boolean laws and realize it using logic gates. 2. Simplify a given POS (3 variable) using Boolean laws and realize it using logic gates.
7	2,4	1,2	<u>Boolean expression simplification using K Map</u> <ul style="list-style-type: none"> • Karnaugh Map: Need, Examples. • Map grouping rules. • Simplification of 2 and 3 variable Boolean expressions using K-map. • Realize the above simplification using logic gates. 	<ol style="list-style-type: none"> 1. Reduce any 4 variable Boolean expressions using K-map. 2. Realize and verify the above simplified Boolean expression using logic gates.
8	3,4	2,3,4	<u>Combinational Circuits: Arithmetic Circuits</u> <ul style="list-style-type: none"> • Features of combinational circuits, applications and examples. • Half adder (HA): Concept, truth-table, logical expression, gate-level implementation. • Full adder (FA): Concept, truth-table, logical expression, gate-level implementation. • Half Subtractor (HS): Concept, truth-table, logical expression, gate-level implementation. • Full Subtractor (FS): Concept, truth-table, logical expression, gate-level implementation. 	<ol style="list-style-type: none"> 1. Construct and Verify Full Adder. 2. Construct and Verify Full Subtractor.

9	3,4	2,3,4	<u>Combinational Circuits: Adders & Comparators</u> <ul style="list-style-type: none"> Serial adders and Parallel adders: Concept, comparison & their applications. Working 8-bit serial adder. 3-bit parallel adder: Concept, Block diagram and its working. 1-bit magnitude comparator: Concept, Block diagram, truth-table, logical expression, gate-level implementation and application. 	<ol style="list-style-type: none"> Implement 3-bit parallel adder using IC 7483. Realize 1 bit comparator using logic gates.
10	3,4	2,3,4	<u>Combinational Circuits: Multiplexers</u> <ul style="list-style-type: none"> Multiplexers (Mux): Concept, general block diagram, No. of inputs to select line calculation. 2:1 Mux: Block diagram, truth-table, logical expression, gate-level implementation. 4:1 Mux: Block diagram, truth-table, logical expression, gate-level implementation. Applications of Mux. 	<ol style="list-style-type: none"> Implementation of 2:1 Mux using logic gates. Verify the functionality of 4:1 Mux using IC 74151.
11	3,4	2,3,4	<u>Combinational Circuits: De-Multiplexers</u> <ul style="list-style-type: none"> De-Multiplexers (De-Mux): Concept, general block diagram, No. of inputs to select line calculation. 1:2 De-Mux: Block diagram, truth-table, logical expression, gate-level implementation 1:4 De-Mux: Block diagram, truth-table, logical expression, gate-level implementation Applications of De-Mux. 	<ol style="list-style-type: none"> Implementation of 1:2 De-Mux using logic gates Verify the functionality of 1:4 De-Mux using IC 74139.
12	3,4	2,3,4	<u>Combinational Circuits: Encoders & Decoders</u> <ul style="list-style-type: none"> 4:2 Encoder: Block diagram, truth-table, logical expression, gate-level implementation, Applications. 2:4 Decoder: Block diagram, truth-table, logical expression, gate-level implementation, Applications. Decimal-to-BCD encoder: Logic diagram, working, truth-table and application. BCD-to-Decimal decoder: Logic diagram, working and truth-table. 	<ol style="list-style-type: none"> Implement 4:2 Encoder using Logic gates. Implement 2:4 Decoder using Logic gates.

13	3,4	2,4	<u>7 - Segment Display</u> <ul style="list-style-type: none"> • Seven-segment display: Principle and types. • Identify and list ICs for 7-segment display and Decoder. • BCD-to-seven segment decoder: Logic diagram, working and truth table (Only Anode Type) 	Implement BCD to 7 Segment decoder using a suitable IC.

NOTE

1. In practice sessions all video demonstrations should be followed by MCQ/Quiz/Subjective questions and evaluation has to be documented.
2. Online course completion certification to be done on relevant topics on Swayam/NPTEL/Infosys Springboard platforms or any other platform.
3. Problems statement to be collected from the relevant industries, resolve and submit it to the course coordinator.

4. References:

- i) Digital fundamentals – Thomas L. Floyd, PEARSON EDUCATION publication, Eleventh edition – Global Edition, ISBN 10: 1-292-07598-8, ISBN 13:978-1-292-07598-3.
- ii) Digital Electronics –principles and integrated circuits. Anil K. Maini. Wiley publications, first edition. ISBN:978-81-265-1466-3.
- iii) Digital principles and applications. Donald P Leach, Albert Paul Malvino, GoutamSaha, McGraw Hill Publisher, 7th edition, ISBN:978-0-07-014170-4.
- iv) Digital Systems-principles and applications. Ronald J. Tocci, Neal S.Widmer, Gregory L. Moss, Prentice Hall Publications, 8th edition, ISBN:0-13-085634-7.
- v) Digital Computer Fundamentals, -Thomas C Bartee, McGraw-Hill Publisher, 4th edition. ISBN 0-07-003892-9.

5. CIE Assessment Methodologies

Sl.No	CIE Assessment	Test Week	Duration (minutes)	Max marks	Average of all CIE=50 Marks
1.	CIE-1 Theory Test	4	90	50	
2.	CIE-2 Practice Test	7	180	50	
3	CIE-3 Theory Test	10	90	50	
4.	CIE-4 Practice Test	13	180	50	
5	CIE-5 Portfolio evaluation of all the activities through Rubrics	1-13		50	
Total					50 Marks

Note: -

Portfolio evaluation includes average of (a) and (b)

- (a) Any one of the suggested activity model with report and presentation evaluated for 50 marks
- (b) Each laboratory exercise will be evaluated for a total of 50 marks. The evaluation will include the following components:

1. Written description of the experiment in the observation book.
2. Conducting the experiment and the associated learning outcomes.
3. The results obtained from the experiment.
4. Corrections and evaluations of the experiment completed in the previous class, documented in the record book.

6. SEE - Theory Assessment Methodologies

Sl. No	SEE - Theory Assessment	Duration	Exam Paper Max marks	Exam Paper Max Marks scale down to (Conversion)	Min marks to pass
1.	Semester End Examination- Theory	3 Hours	100	50	20

7. CIE Theory Test model question paper

Program	Electronics and Communication Engg.			Semester -1	
Course Name	Digital Electronics-I			Test	I/III
Course Code		Duration	90 min	Marks	50
Name of the Course Coordinator:					
Note: Answer any one full question from each section. Each full question carries equal marks.					
Q.No	Questions	Cognitive Level	Course Outcome	Marks	
Section - 1					
1	a) Choose any 3 Analog signals and any 2 Digital signals from real environment	L3	CO1	05	
	b) Convert the given Binary to Hexadecimal and a given Hexadecimal to Binary	L3	CO1	5+5	
	c) Convert the given Binary to Gray and the given Gray to Binary	L3	CO1	5+5	
2	a) Chart main advantages of digital signals over analog signals?	L3	CO1	05	
	b) Convert the given Decimal to Hexadecimal and a given Hexadecimal to Decimal.	L3	CO1	5+5	
	c) Perform addition of the given 4-bit binary number and subtraction of the given 4 bit binary number.	L3	CO1	5+5	
Section - 2					

3	a) Mention and explain any 5 Boolean laws in Boolean algebra.	L2	CO2	5
	b) Create a truth table for a 3-input AND gate and OR gate.	L2	CO2	10
	c) Realize the basic logic function using only NAND or NOR gates.	L3	CO2	10
4	a) State and Interpret De-Morgan's theorem.	L2	CO2	5
	b) Express basic logic gates using only NAND gate?	L2	CO2	10
	c) Simplify the given Boolean expression and implement using suitable Logic gates.	L3	CO2	10

Note for the Course coordinator:

1. Each question may have one, two or three subdivisions. Optional questions in each section carry the same weightage of marks, cognitive level and course outcomes. All questions must be framed under Understand (L2) & Apply (L3) cognitive level using Revised Bloom's Taxonomy.

Signature of the
Course Coordinator

Signature of the
HOD

Signature of the
IQAC Chairman

8. CIE Practice Test model question paper

Program	Electronics and communication Engineering			Semester	1
Course Name	Digital Electronics-1			Test	II/IV
Course Code		Duration	180 min	Marks	50
Name of the Course Coordinator:					
Questions				CO	Marks
Write-up for two experiments and conduction of any one experiment.					50
Scheme of assessment					
a) Writing the Circuit diagram, tabular column, calculations etc. for two experiments.					20
b) Rig up and Conduction of any one					15
c) Result					05
d) Viva-voce					10
Total Marks					50

Signature of the
Course Coordinator

Signature of the
HOD

Signature of the
IQAC Chairman

9. Suggestive Activities for students:

The List is an Example and not inclusive of all possible activities of the course. Students and Faculty are encouraged to choose activities that are relevant to the topic.

Note: Activity can be undertaken by either an individual or a team comprising up to 5 students.

Sl.No.	Suggestive Activities for students
01	Designing a Simple Digital lock. To design and implement a digital lock using combinational logic that requires a specific 3-bit binary code to unlock. Components: * 7404 (NOT Gate IC) * 7408 AND Gate IC * 7432 (OR Gate IC) * 7486 (XOR Gate IC) * Breadboard, jumper wires, logic switches, LEDs, resistors.
02	Designing a Simple Parity Checker. To design a simple parity checker using combinational logic that determines whether a binary number has even or odd parity. Components: * 7404 (NOT Gate IC) * 7408 (AND Gate IC) * 7432 (OR Gate IC) * Breadboard, jumper wires, logic switches, LEDs, resistors
03	Designing a Simple 4-bit BCD Adder. To design and implement a 4-bit Binary-Coded Decimal (BCD) adder that adds two 4-bit BCD numbers and produces a BCD result. Components: * 7404 (NOT Gate IC) * 7408 (AND Gate IC) * 7432 (OR Gate IC) * 7486 (XOR Gate IC) * Breadboard, jumper wires, logic switches, LEDs, resistors
04	Designing a Simple Binary-to-Decimal Converter. To design and implement a binary-to-decimal converter using combinational logic that converts a 4-bit binary number to its decimal equivalent, displaying the result on LEDs. Components: * 7404 (NOT Gate IC) * 7408 (AND Gate IC) * 7432 (OR Gate IC) * 7447 (BCD to 7-segment Decoder IC) or equivalent * 7-segment displays (if using a BCD decoder) * Breadboard, jumper wires, logic switches, resistors.
05	Designing a Simple 4-bit Binary Alarm System. To design and implement a basic 4-bit binary alarm system that triggers an alarm when a specific 4-bit binary code is entered. Components: 7404 (NOT Gate IC) 7408 (AND Gate IC) 7432 (OR Gate IC) 7486 (XOR Gate IC) Breadboard, jumper wires, logic switches, buzzer or LED (for alarm), resistors.

10. Rubrics for Assessment of Activity (Qualitative Assessment)

Sl. No.	Dimension	Beginner	Intermediate	Good	Advanced	Expert	Students Score
		10	20	30	40	50	
1		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	40
2		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	30
3		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	50
4		Descriptor	Descriptor	Descriptor	Descriptor	Descriptor	20
Average Marks=(40+30+50+20)/4=35							35

Note: Dimension and Descriptor shall be defined by the respective course coordinator as per the activities

11. Equipment/software list with Specification for a batch of 30 students

Sl.No.	Particulars	Specification	Quantity
01	Digital trainer kits.		15
02	IC tester, logic probes.		05
03	Digital Multimeters		15
04	Suitable ICs		20 Each
05	Patch cards (Different lengths)		300

